REMARKS

Claims 1-13 and 21-26 are pending in the application.

Claims 1-13 and 21-26 are rejected.

Claims 21-26 are rejected under 35 U.S.C. 112.

Claims 1, 4, 8 and 11 are rejected under 35 U.S.C. 102(e).

Claims 2-3, 5-7, 9-10, 12-13 and 21-26 are rejected under 35 U.S.C. 103(a).

Claim 2 is cancelled.

Claims 1, 3, 21, 25 and 26 are amended.

No new matter is added.

Claims 1, 3-13 and 21-26 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Rejections – 35 U.S.C. § 112

Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The rejections are respectfully traversed.

With respect to amended independent claim 21, the claim is amended to clarify that the first and second chip scale packages each have a matrix of ball land pads that are the same size. As noted in the specification at page 6, lines 24-29, "the matrix of ball land pads 163 of the upper chip scale package 150 is the same as that of the lower chip scale package 110." By keeping these matrices the same size, "an addition of a new chip scale package to the stack package is easily accommodated because each chip scale package used for the stack package is standardized."

With respect to amended claims 25 and 26, these claims are amended to clarify that a third and a fourth chip scale package each include a matrix of ball land pads that is the same size as the first and second matrices of ball land pads.

Claim Rejections – 35 U.S.C. § 102

Claims 1, 4, 8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pub. 2002/0124518 to Karnezos. The rejections are respectfully traversed.

With respect to amended claim 1, the claim is amended to include the limitations of claim 2 and to further clarify that the connecting board is attached to the circuit patterns on the lower surface of the substrate of the upper stacked chip and the circuit patterns on the

lower surface of the substrate of the lower stacked. This is supported within the specification at page 5, lines 11-18 and in FIGS. 4-6.

As the Examiner notes with respect to claims 2-3, 5-7, 9-10, 12-13 and 21-26, Karnezos does not disclose electrically connecting the upper chip package and lower chip package by connecting boards. Thus, Karnezos fails to disclose each and every element of amended independent claim 1. Therefore, claim 1 is believe to be allowable over Karnezos and allowance is respectfully requested.

As will be explained below, even if Karnezos is combined with Cha, the combination still fails to disclose each and every element of amended claim 1.

Claims 4, 8 and 11 all depend from amended independent claim 1 and for at least the reasons given for claim 1, these claims are believed to be allowable and allowance is respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 2-3, 5-7, 9-10, 12-13 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. 2002/0124518 to Karnezos in view of U.S. Pub. 2004/0150107 to Cha, et al. The rejections are respectfully traversed.

Claim 2 is cancelled. Claims 3, 5-7, 9-10 and 12-13 all depend from amended independent claim 1. Claim 1 is amended to include the limitations of claim 2 and to clarify that the connecting board is attached to the circuit patterns on the lower surface of the substrate of the upper stacked chip and to the circuit patterns on the lower surface of the substrate of the lower stacked chip. As noted above, the amended language is supported within the specification at page 5, lines 11-18 and in FIGS. 4-6.

The Examiner notes that Karnezos does not disclose electrically connecting the upper chip package to the lower chip package by a connecting board. Cha is cited as disclosing a connecting board connecting an upper and a lower chip package. Cha, however, does not disclose attaching a connecting board to circuit patterns on the lower surface of the substrate of either the upper or lower chips. Cha, at paragraph [0078] discloses connecting the flexible substrate 120 to the solders balls 4 that are inserted into the holes 132 in the flexible substrate.

FIGS. 12a-c and 13 in Cha also show a flexible substrate 320A. The flexible substrate 320A, however, is attached to the solder balls 4 of the upper chip package 310A and to the upper surface of the substrate of the lower chip package 310B. Further, FIG. 14 in Cha shows a flexible substrate 320A connecting upper package 310A to lower package 310B. The

flexible substrate 320A in FIG. 14, however, attaches to the ball land pads of the upper package 310A and not to any circuit patterns on the lower substrate of the upper package. (See paragraph [0131]).

Thus, Karnezos in view of Cha also fails to present a *prima facie* case of obviousness with respect to amended independent claim 1. Because claims 3, 5-7, 9-10 and 12-13 all depend from claim 1, for at least the same reasons as given for claim 1, Karnezos in view of Cha fails to present a *prima facie* case of obviousness with respect to these claims. Therefore, claims 3, 5-7, 9-10 and 12-13 are believed to be allowable and allowance is respectfully requested.

With respect to amended independent claim 21, the claim is amended to clarify that the first and second chip scale packages have, respectively, first and second matrices of ball land pads that are the same size matrix. Support for this amendment is found at page 5, lines 23-29 of the specification. Also, the claim recites that the lower surfaces of the first and second chip scale packages face the opposite direction.

Karnezos only discloses in FIGS. 5-11 that the matrix of ball land pads on the upper chip package is smaller than the matrix of ball land pads on the lower chip scale package. The stack package disclosed by Karnezos must have this configuration because Karnezos only discloses connecting the upper and lower packages using wires 518 (see FIG. 5A). For the wires 518 to be protected within the encapsulant 507, the lower matrix is necessarily bigger than the upper matrix.

Cha does not disclose chip scale packages that have the lower surface of the substrates facing in opposite directions. Further, there is no disclosure within Cha or Karnezos enabling one to stack and connect packages with the lower surfaces of the substrates facing in opposite directions in the manner claimed.

Thus, Karnezos in view of Cha fails to present a *prima facie* case of obviousness with respect to amended independent claim 21. Therefore, claim 21 is believed to be allowable and allowance is respectfully requested.

Claims 22-26 all depend from claim 21, and for at least the reasons given for claim 21, these claims are believed to be allowable and allowance is respectfully requested.

For the foregoing reasons, reconsideration and allowance of claims 1, 3-13 and 21-26 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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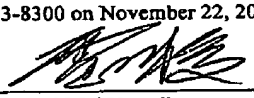

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